MODULE SPECIFICATION

Code: UFEEHH-30-2	**Title: CPU Architecture & VHDL**	**Version: 2008**
Level: 2	**UWE credit rating: 30**	**ECTS credit rating: 15**
Module Type: Standard		
Owning Faculty: Bristol Institute of Technology	**Field: Design and Engineering**	
Valid from: 1st September 2008	**Discontinued From: 31st August 2009**	
Pre-requisites:	**UFEE73-30-1 Digital Design & Instrumentation OR UFEE7B-20-1 Digital Electronics OR UFEETT-20-1 Digital Design and Instrumentation**	
Co-requisites:	**None**	
Excluded combinations:	**None**	

Learning Outcomes

On completion of this module a student will typically be able to:-		*Assessed in component(s):*
A. Show a detailed knowledge and understanding of		
i)	high level language approaches to hardware design as an alternative to the more traditional embedded system/microbased system approach	A, B
ii)	how software design principles can be applied to hardware design	A, B
iii)	some of the current design and development techniques used in the development of systems on silicon	A, B
B. Demonstrate subject specific skills with respect to		
i)	the use of CPLDs, FPGAs and ASICs as targets for VHDL	A, B
ii)	the detailed architecture and functionality of a simple processor	A, B
iii)	the understanding and use of system simulation in preliminary phases of system design	A, B
iv)	the use of the VHDL language and confidence in both structural and behavioural approaches	A, B
C. Show cognitive skills with respect to		
i)	applying appropriate design techniques to a range of problems	A, B
ii)	an understanding of the advantages and disadvantages of the use of Hardware Description Languages	A, B

D. Demonstrate key transferable skills in

i)	communication skills	A, B
ii)	self-management skills	B
iii)	IT skills in context	B
iv)	problem formulation and decision making	A, B
v)	working with others	B

Syllabus Outline

CPU architecture, the basic components and functionality

Parallel adders/subtractors, and multipliers, barrel shifters

VHDL modelling concepts, overview

The Dataflow/RTL model

The Structural Model

VHDL State machines

VHDL Subsets for synthesis

Design Processing

Test patterns and Simulation.

Digital Design principles

Optimisation of designs

Timing hazards

CMOS implementation of logic

Combinational Logic design Principles

Sequential Design Principles.

State machine synthesis

Use of diagrammatic tools for code synthesis

Synthesis Issues

Programmable devices, structure and function.

Synthesis process, download, testing and debugging in hardware

Developing tool chains, ancillary utilities. Use of Make, Flex etc.

Teaching and Learning Methods

This module will be presented through a combination of lectures and practicals. The practicals will provide the students with access to a VHDL development system for introductory experimentation and project work.

Individual worksheet and group-oriented practical exercises are central to the students\' experience in order to reinforce and extend the lectures and associated readings. The laboratory work includes both hardware and software, at basic unit and higher system level.

An extended case-study, supported by focussed tutorials and practicals, will allow the students to follow through an example application from design to implementation, and appreciate the relevance of all the component parts of the module syllabus. Examples of case studies could be: the design and emulation of a \'set top\' recorder such as the TiVo and the development of a custom microcontroller for remote data capture systems.

Indicative Reading List

The following list is offered to provide validation panels/accrediting bodies with an indication of the type and level of information students may be expected to consult. As such, its currency may wane during the life span of the module specification. However, CURRENT advice on readings will be available via other more frequently updated mechanisms.

Zwolinski M (2000). *Digital system design with VHDL,* Prentice Hall

Carpinelli J D (2001). *Computer Systems Organization & Architecture,* Addison Wesley

Wakerly J F (2000). *Digital Design Principles & Practice 3rd Ed.*, Prentice Hall

Ashenden P J (1998). *The Students guide to VHDL,* Morgan Kaufmann Publishers

Assessment

Weighting between components A and B A: 25% B: 75%

ATTEMPT 1
First Assessment Opportunity

Element Description	**% of Component**	**% of Assessment**
Component A (Controlled Conditions)		
Examination	100%	25%
Component B		
Coursework	100%	75%